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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,223	06/13/2001	Louis L. Hsu	728-208(YOR9-2001-0270 US	5309
7590 07/28/2004			EXAMINER	
Paul J. Farrell, Esq. DILWORTH & BARRESE LLP 333 Earle Ovington Boulevard Uniondale, NY 11553			RAO, SHRINIVAS H	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/880,223

Applicant(s)

HSU ET AL.

Examiner

Steven H. Rao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 12 and 14-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 12 and 14-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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***Response to Amendment***

Applicants' amendment filed on May 17, 2004 has been entered on May 23, 2004.

Therefore claim 12 as amended by the amendment and The examiner's amendment below and claims 14-17 as previously filed are currently pending.

Claims 1-11,13 and 18 –31 were previously cancelled.

**Examiner's Amendment**

During a telephone interview with Jeffery Kirshner on Thursday July 15, 2004 , Mr. Krishna authorized Ex. Rao to delete, " formed in a polysilicon layer " in line 5 of claim 12.

It is noted that " formed in a polysilicon layer" was suggested as alternative language if supported by the specification to attempt to overcome the 112 rejections.

It is noted that Applicants' specification page 7 lines

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12, 14 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

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Claim 12 recites, "wherein said transfer gate covers the entire top surface of said thyristor" is not supported by the specification as originally filed.

The written description does not contain disclosure that the horizontally stacked pseudo-TFT transfer gate as covering the entire top surface of the PNP thyristor 212.

The drawing figures do not show the horizontally stacked pseudo-TFT transfer gate ( identified as numeral 220 in Figure 13) as covering the entire top surface of the PNP thyristor 212, rather the drawings show a gap between WLL2 and the end of the horizontally stacked pseudo-TFT transfer gate above region 120 C in figure 13 .

The previous rejection also contained this rejection and specifically stated that the previous rejection was based on the assumption *arguendo*

"Assuming *arguendo* that the newly added limitation, " wherein said thyristor being buried underneath said transfer gate, wherein said transfer gate covers the entire top surface of said first device, and further wherein the top surface of said transfer gate forms a planar top surface of each said transfer gate of each of said T-Ram cell." is supported by the specification as originally filed the following rejection is made."

Applicants' reference to figure 13 in their remarks section is inadequate to overcome the rejection and does not provide any support in the original specification to show that the horizontally stacked pseudo-TFT transfer gate ( identified as numeral 220 in Figure 13) as covering the entire top surface of the PNP thyristor 212.

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,448,586 to Nemati et al. ( herein after Nemati) in view of Kumagi ( U.S. Patent .No. 5,357,125 herein after Kumagi) both previously applied . For response to Applicants' arguments see section below.

With respect to claim 12, a T-Ram array including a plurality of T-Ram cells arranged in an array ( Nemati fig. 8, col. 6 lines 65-66), wherein each of the plurality of T-Ram cells includes a buried vertical thyristor region beneath at least a portion of a transfer gate region. ( Nemati fig.8, p portion of 40 a, b, and c under respective gate 48).

Nemati does not label his gate as a transfer gate however it is inherent from the description in col. 7 lines 1-15 that Nemati's gate 48 functions like a pseudo TFT ( similar to applicant's description at page 5 of the specification ) and therefore one of ordinary skill in the art would readily recognize Nemati's gate 48 to be a transfer gate similar to that claimed.

The remaining limitations of claim 12 are :

And a horizontally stacked pseudo-TFT transfer gate , ( see above) , said transfer gate (i.e. pseudo TFT) including a source/drain and body ( Nemati col. 5 lines 46 to 61) .

Assuming arguendo that the newly added limitation, " wherein said thyristor being buried underneath said transfer gate, wherein said transfer gate covers the entire top surface of said first device, and further wherein the top surface of said transfer gate forms a planar top surface of each said transfer gate of each of said T-Ram cell." is supported by the specification as originally filed the following rejection is made.

Nemati does not specifically describe the newly added limitation wherein said second device being buried underneath said second device, wherein said second device covers the entire top surface of said first device, and further wherein the top surface of said transfer gate forms a planar top surface of each said transfer gate of each of said T-Ram cell.

However, Kumagi in figures 1-5 and col. 5 lines 61-68 and figures 2 and 5 describes wherein said second device being buried underneath said second device, wherein said transfer gate covers the entire top surface of said thyristor , and further wherein the top surface of the transfer gate forms a co-planar top surface of each said transfer gate of each of said T-Ram cell to form a semiconductor device that is readily integrated into one chip and can be effectively used as a power switching device.

Therefore it would have been obvious to one of ordinary skill in the art to include Kumagi's said thyristor buried underneath said transfer gate, wherein said transfer gate covers the entire top surface of said thyristor , and further wherein the top surface of the transfer gate forms a co-planar top surface of each said transfer gate of each of said T-Ram cell and wherein Nemati's device to form a semiconductor device that is

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readily integrated into one chip and can be effectively used as a power switching device.

With respect to claim 14, wherein each of the plurality of cells has a size less than or equal to  $8F^2$ . ( It is well known in the prior art that T-ram cells have a size of  $8F^2$  or less as admitted by the applicants' herein in their co-pending application No.2002/0093030 published on July 18, 2002 in its abstract lines 10 –13 etc.)

With respect to claim 15, wherein said substrate is a semiconductor SOI or bulk wafer ( Neamti fig. 6a # col. 6 lines 20-27).

With respect to claim 16, wherein the base of said thyristor is surrounded by a surround gate . ( Nemati fig. 8 thyristors 40 a, b and c being surrounded by the gate 48).

With respect to claim 17, Nemati describes wherein each of the plurality of T-Ram cells includes structure for the traversal of at least two word lines there through. ( Nemati fig. 5, col. 5 lines 33-60) said planar top surface of each T-Ram cell provides for simplified fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-Ram cells, said wirings for inter connecting said T-Ram cells .

The limitation , "said planar top surface of each T-Ram cell provides for fabrication of metal wirings, said wirings being fabricated over said planar top surface of said T-Ram cells, said wirings for inter connecting said T-Ram cells " is taken to be a product by process limitation.

### ***Response to Arguments***

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Applicant's arguments filed 5/17/ 2004 have been fully considered but they are not persuasive for the following reasons:

Applicants' first contention that Nemati does not disclose a stacked pseudo-TFT transfer gate but rather discloses a control gate ( i.e. #48) is not persuasive because Nemati as previously stated in figure 6 and col. 5 lines 61 –65 states its element 48 is a stacked psuedo TFT.

FIG. 6 illustrates an alternative implementation to that which is shown in FIG. 1. The structures of FIGS. 1 and 6 differ in that the structure of FIG. 6 includes a vertically-arranged NMOSFET 30 instead of the NMOSFET 12 of FIG. 1, which is arranged in a planar manner relative to the P substrate. The NMOSFET 30 includes a gate 14' that at

Applicants' arguments of 8/11/ 2003 namely, " In contrast, it is inherent in a pseudo\_TFT gate as recited in claim 12 as amended that both the source/ drain and the body are contained in a polysilicon layer. " was not purasive because the same was not recited in the claim 12 till applicants' amendment of 1/23/ 2004, and therefore Applicants' arguments were not consumerate in scope with their arguments .

Applicants' amendment of 1/23/2004 again has 112 problems because claim1 2 presently recites " said transfer gate including a source/drain and body formed in a polysilcicon layer ". It is understood by one skilled in the art that a gate does not include a source/drain and body regions , but that a pseudo-TFT may include the source/drain and body regions, assuming this is what Applicants' meant , all the added limitations are taught by Nemati col. 5 lines 46 to 61.

Dependent claims 14-16 and (17) were alleged to be allowable as they depend upon allegedly allowable claim 12.



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However as shown above claim 12 is not allowable. Therefore claims 14-17 as also not allowable.


Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 8:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

July 21, 2004.

  
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